CLAIMS

What is claimed is:

1. A method of processing a request in a computer system, comprising the acts of:

(a) initiating a read request from a requesting agent, the requesting agent residing on a bus, wherein the read request has an address corresponding to a memory location;

(b) receiving the read request at a processor controller;

(c) sending the read request from the processor controller to an access controller;

(d) sending a deferred reply from the processor controller to the requesting agent when the processor controller is free to process the read request;

(e) delivering data residing at the address corresponding to the memory location to the access controller;

(f) delivering the data from the access controller to the processor controller; and

(g) delivering the data from the processor controller to the requesting agent.

2. The method of processing a request, as set forth in claim 1, comprising the act of sending a data ready signal from the access controller to the processor controller upon receipt of the data at the access controller.

3. The method of processing a request, as set forth in claim 1, wherein act (a) comprises the act of initiating a read request from a processor residing on a processor bus.

4. The method of processing a request, as set forth in claim 1, wherein act (a) comprises the act of initiating a read request from a peripheral device residing on an input/output (I/O) bus.

5. The method of processing a request, as set forth in claim 1, wherein act (c) comprises the act of sending the request from the processor controller to a memory controller.

6. The method of processing a request, as set forth in claim 1, wherein act (c) comprises the act of sending the request from the processor controller to a tag controller.

7. The method of processing a request, as set forth in claim 1, wherein act (d) comprises the act of sending a deferred reply immediately upon the agent bus being available to receive data from the memory location.

8. The method of processing a request, as set forth in claim 1, wherein act (d) comprises the act of waiting a predetermined number of clock cycles after the deferred reply is sent before delivering data.

9. The method of processing a request, as set forth in claim 1, wherein acts (d) and (f) are performed simultaneously.

10. The method of processing a request, as set forth in claim 1, wherein the acts are performed in the recited order.

11. A method of processing a request in a computer system, comprising the acts of:

(a) sending a request from a processor controller to an access controller on a first clock cycle, the request originating from an agent; and

(b) sending a deferred reply from the processor controller to the agent on a second clock cycle, the second clock cycle being immediately subsequent to the first clock cycle.

12. The method of processing a request, as recited in claim 11, wherein act (a) comprises the act of sending a request from a processor controller to a memory controller on a first clock cycle.

13. The method of processing a request, as set forth in claim 11, wherein act (a) comprises the act of sending a request for a processor controller to a tag controller on a first clock cycle.

14. A method of processing a request in a computer system, comprising the acts of:

(a) asserting a first request signal from a host controller during a first clock cycle, wherein the first request signal is configured to block requests from all agents to the host controller;

(b) asserting a second request signal from the host controller during a second clock cycle, the second clock cycle being immediately subsequent to the

first clock cycle, and wherein the second request signal is configured to block requests from external agents only to the host controller; and

(c) de-asserting the first request signal.

15. The method of processing a request, as set forth in claim 14, wherein act (a) comprises the act of asserting a first request signal from the host controller upon detecting that one or more queues residing internally with respect to the host controller is full.

16. The method of processing a request, as set forth in claim 14, wherein act (a) comprises the act of asserting a block next request (BNR) signal.

17. The method of processing a request, as set forth in claim 14, wherein act (b) comprises the act of asserting a second request signal from the host controller upon anticipating that a transaction should be run within the host controller to clear one or more queues residing internally with respect to the host controller.

18. The method of processing a request, as set forth in claim 14, wherein act (b) comprises the act of asserting a bus priority request (BPRI) signal.

19. A computer system comprising:

a plurality of buses;

a memory system operably coupled to the plurality of buses; and

a processor controller coupled to each of the plurality of buses and configured to simultaneously issue a deferred reply to a requesting device in response to receiving a read request from the requesting device and obtain the data corresponding to the read request from the memory system.

20. The computer system, as set forth in claim 19, wherein at least one of the plurality of buses comprises a processor bus.

21. The computer system, as set forth in claim 19, wherein at least one of the plurality of buses comprises an input/output (I/O) bus.

22. The computer system, as set forth in claim 19, wherein the processor controller is further configured to obtain the data corresponding to the read request from the memory system before issuing a deferred reply to a requesting device.

23. The computer system, as set forth in claim 19, wherein the memory system comprises a redundant memory system.

24. A computer system comprising:

a plurality of buses;

a memory system operably coupled to the plurality of buses; and

a processor controller coupled to each of the plurality of buses and configured to assert a first request signal during a first clock cycle, wherein the first request signal is configured to block requests from all agents to the processor controller, and wherein the processor controller is configured to assert a second request signal during a second clock cycle, the second clock cycle being immediately subsequent to the first clock cycle, and wherein the second request signal is configured to block requests from external agents only to the processor controller.

25. The computer system, as set forth in claim 24, wherein at least one of the plurality of buses comprises a processor bus.

26. The computer system, as set forth in claim 24, wherein at least one of the plurality of buses comprises an input/output (I/O) bus.

27. The computer system, as set forth in claim 24, wherein the processor controller is configured to assert a block next request (BNR) signal during the first clock cycle.

28. The computer system, as set forth in claim 24, wherein the processor controller is configured to assert the second request signal upon anticipating that a transaction should be initiated to clear one or more queues in the computer system.

29. The computer system, as set forth in claim 24, wherein the processor controller is configured to assert a bus priority request (BPRI) signal during the second clock cycle.